B.E. / B.Tech. Electronics & Communication/Telecommunication Engineering (Model Curriculum)
Semester-VI

ET601M3 / CMOS1 - Program Elective-II - CMOS Design

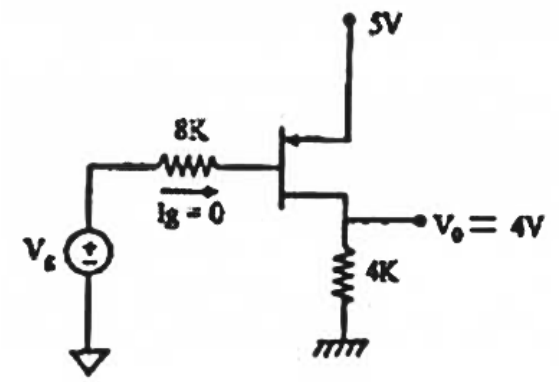
P. Pages : 2 **GUG/S/25/13930**

Time : Three Hours * 2 3 4 0 * Max. Marks : 80

Notes : 1. All questions carry marks as indicated.
2. Due credit will be given to neatness and adequate dimensions.
3. Assume suitable data wherever necessary.
4. Illustrate your answers wherever necessary with the help of neat sketches.

1. a) Define Channel length modulation? Derive an expression for I_{DSAT} and channel length modulation coefficient. **8**

b) For the PMOS circuit shown in the figure Find the value of I_D and V_{DS}; Given : $K = 0.25\ mA / v^2$; Vth = -2V. **8**



OR

2. a) Write a note on IC technology. **4**

b) Distinguish between enhancement mode and depletion mode MOSFET. **6**

c) Elaborate the action of enhancement type MOSFET for different values of Vgs. **6**

3. a) Discuss in detail about following technique used in producing silicon-on-insulator (SOI) technology. **8**
i) Hetro-epitaxial technique.
ii) Homo-epitaxial technique.
iii) Re crystallization technique.

b) Obtain the DC transfer characteristic of CMOS inverter and mark all the regions showing the status of NMOS and PMOS. **8**

OR

4. a) Differentiate between λ-based design rules and μ-based design rules. **4**

b) Design CMOS inverter with the help of stick diagram and physical layout. (use λ based design rules) **6**

c) Explain the operation of Bi-CMOS Inverter. **6**

5. a) How transistor scaling is done? Discuss its effect. **8**

b) Write a short note on:- **8**
i) Latch up problem in CMOS.
ii) Soft error.

OR

6. a) Derive an expression for short circuit dissipation for CMOS. **8**

b) Find the scaling factor for (i) Channel Resistance (ii) Current Density. **8**

7. a) Implement the following Boolean function using transmission gate **6**

$$F = AB + A'C' + AB'C$$

b) Design NAND and NOR gate by using CMOS along with its stick diagram and physical layout. (for drawing physical layout use λ based design rules) **10**

OR

8. a) Define Euler's path. Implement the Boolean equation **8**

$$Z = \overline{A.(D+E)+B.C}$$

Using Euler's path and draw its equivalent stick diagram and physical layout structure.

b) Implement 4:1 Mux using transmission gate. **8**

9. a) Implement CMOS D-Latch using proper schematic diagram. **8**

b) Explain in detail conventional CMOS flip-flops. **8**

OR

10. a) Write a note on resettable Latches and Flip Flops. **8**

b) Design CMOS JK Flip Flop by using NOR gate and NAND gate. **8**

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